The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD B. WATSON JR., SEAN MICHAEL WELCH, OSCAR MENDOZA and DAVID F. BERTUCCI

Appeal No. 2006-1212
Application 10/655,321

ON BRIEF

Before THOMAS, HAIRSTON, and MACDONALD, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appeal to the Board from the examiner's final rejection of claims 19, 20, 23, 24, 45, 49, 50, 63 and 65. The examiner has objected to claims 64 and 66 and has allowed claims 27, 28, 32 through 34 and 62.

Representative claim 45 is reproduced below:

45. A method for determining an uncertainty window within which a target clock signal of an electronic device makes states transitions, the method comprising:

generating on a microprocessor die a first, second, third and fourth reference clock signals having the same frequency but differing in phase relationship;

defining a first time bin between respective features of the first and second reference clock signals, defining a second time bin between respective features of the second and third reference clock signals, and defining a third time bin between respective features of the third and fourth reference clock signals;

comparing on the microprocessor die a plurality of cycles of the target clock signal to the reference clock signals to determine in which bin the target clock signal makes it state transitions;

adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin; and

repeating the adjusting and the comparing until the uncertainty window is determined.

The following reference is relied on by the examiner:

Kelkar et al. (Kelkar) 5,663,991 Sept. 2, 1997

Claims 19, 20, 23, 24, 45, 49, 50, 63 and 65 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kelkar.

Pages 2 and 3 of the answer make clear that the examiner has withdrawn a preexisting rejection under 35 U.S.C. § 103 of claims 27, 28, 32 and 66.

Rather than repeat the positions of the appellants and the examiner, references is made to the brief and reply brief for appellants' positions, and to the answer for the examiner's positions.

OPINION

For the reasons set forth by the examiner in the answer, as embellished upon here, we sustain the rejection of all claims on appeal under 35 U.S.C. § 102. Beginning at page 17 of the brief, appellants present arguments only as to claim 45 which is characterized here as representative of all the claims on appeal.

Appellants' figure 1B shows a clock skew 10 and duty cycle jitter 18. What appellants have characterized as an "uncertainty window" is shown as element 26 in figure 1C. It is within this window that a state transition, a rising or falling edge, of a clock signal may occur. It is also characterized as the span of time within which clock signals may make a transition. The disclosed and claimed invention desires to measure the target or measured clock signal "uncertainty window" caused by skew and jitter.

In the examiner's statement of the rejection portion of the answer the examiner details what teachings of Kelkar pertains to argued independent claim 45 at pages 4 and 5 of the answer. Even a brief review of the abstract and the summary of the invention at column 2 of Kelkar reveals a correspondence of similar features, particular those of independent 19 on appeal. As the title of Kelkar reveals, the invention in his patent relates to a built in self measurement capability on an integrated circuit chip to measure and adjust for jitter and phase error. This is otherwise characterized as jitter, delays or jitter delays in the discussion in this reference. The overall circuit in figure 1 is described in flow chart functional form in figure 4 of Kelkar. Inasmuch as the examiner makes reference to reference clock signals, they are shown in phased delay form as delay clocks 36 through 42 from an initial reference clock 22 in figure 3. Correspondingly, time slices 46 through 54 correspond to the claimed time bins which correspond to the disclosed time bin in figure 9 illustrated as elements 230A-C. The showing in figure 3 of Kelkar has corresponding time slices 46 through 54.

In a manner corresponding to the claimed determined uncertainty window, it appears that the examiner has noted a corresponding feature is disclosed in Kelkar although it is not well explained by the examiner. From our perspective it appears like the teaching at column 2, lines 30 through 32 and the corresponding discussion at column 5, lines 1 and 2 and the more detailed discussion beginning at line 30 detail a so-called peak-to-peak jitter defined as the maximum difference between two clock edges of an output signal or twice a given time slice within Kelkar. Thus, the reference clearly appears to have corresponding teachings in other words to that which are claimed.

Appellants' arguments beginning at page 17 as to the rejection of claim 45 focus only on the clause "adjusting the phase relationship of at least one of the reference clock signals, and thereby adjusting the time width of at least one time bin." The examiner's corresponding analysis and reliance upon the showing in figure 5 and the discussion of that figure beginning at the last half of column 5 through the end of the reference clearly corresponds to the adjustability of the time width of at least one of the time bins or time slices within Kelkar. The feedback loop shown in figure 5 works in a dynamic

manner to cause an increase in the inverter delay shown in this figure or, alternatively, a decrease in the inverter delay as variably controlled by the delay control signal 85. The variability is described to be correctable based upon variations and processes of manufacture, temperature and power supply voltages as relied upon by the examiner, column 6, lines 28 through 35. Therefore, in the context of the earlier discussion of the peak-to-peak jitter being twice the time slices of Kelkar, it appears to us that the artisan would well appreciate that there is an adjustment of the time width of at least one time bin or time slice as claimed. Appellants' arguments at pages 17 through 20 of the brief are unpersuasive because they appear to focus so much upon argued specification teachings rather than the actual language of the claims.

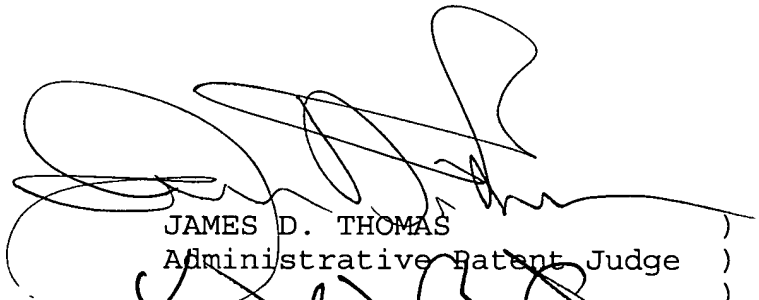
Finally, we note that the examiner addresses these latter arguments at pages 6 and 7 of the answer. In response to positions taken by the examiner in the final rejection, appellants' remarks in the brief are noted by the examiner at page 7 of the answer. The examiner closes his remarks by stating "while changing the frequency of the test clock signal would not be reasonable in this situation, the time slices are adjusted to

compensate for process variations as shown above." The reply brief in turn only quotes for our review the (first or) dependent clause of this sentence and incompletely makes reference to the examiner's independent (or second) clause in this sentence by stating that the examiner merely attempts to rely on Kelkar's adjustment to compensate for processes variations as discussed at pages 1 and 2 of the reply brief. Since the examiner has stated "the time slices are adjusted to compensate for process variations as shown above" as we quoted earlier, appellants' arguments are unpersuasive of any error in the examiner's position. As explained earlier, what Kelkar teaches as adjusting the time slices clearly corresponds to the teachings of adjusting the time width of at least one time bin as recited in independent claim 45.

Since no arguments are presented as to independent claims 19, 63 and 65 on appeal, the rejection of them and their respectively rejected dependent claims is sustained as well. We note in passing that the subject matter of claims 19, 63 and 65 is substantially broader than the more specific recitations argued in independent claim 45. Therefore, in view of the foregoing, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 102 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED



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